Using the Silicon Laboratories' Si4133 RF Synthesiser Chip

By Doug VK4ADC

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A few months back, I became aware of the Si4133 series synthesiser chips after details were posted on the **VKLogger.com** (http://www.vklogger.com/) Forum and having already experimented with the Siemens TBB206G and Melexis TH71221 series devices, I considered using this style for some future UHF local oscillator (LO) use. Graham VK3XDK has already produced LO PCBs (around \$AUD100 at the moment) using this chip to go along with his transverter boards so the outcome/results should be technically sound - but I often like to dig a bit deeper and do things my way. A bit of experimentation is always good as a diversion from other more mundane tasks around the house..

The data sheet is readily available at the **silabs.com web site** (http://www.silabs.com/support/pages/support.aspx? ProductFamily=RF+Synthesizers) and it is very important to also download and read through the Application Notes and the FAQ documents. The chip itself is available in two styles, the 24 pin TSSOP layout (Si4133-GT) or the 28 pin QFN layout (Si4133-GM). They operate at a nominal +3 volts DC supply (maximum rating of +4V) so care has to be taken not to operate with too high a supply voltage (e.g. +5V..).

They aren't too cheap (about \$15 each from **X-ON** (http://www.x-on.com.au/results-new.asp?sq=si4133&tp=) at the moment, plus \$15 freight charge for orders under \$200, takes up to 2 weeks) but they may be a solution to oscillator phase noise noted with the other chip applications. For a few dollars worth of experimentation, they are well worth the effort.

A WORD OF WARNING : There is an eBay supplier (Sisitronic) currently selling Si4133**G**-GT chips at around \$US6.50 each **but** the "G" suffix indicates a special version - one that has an internal R divider set at 65 (and not re-programmable). Great for some specific applications but as a general-purpose synthesiser, these are best avoided.

Ordering in	normat	08:
See po	ige 31.	
Pin Anni Si41:	3-GT	_
800 T 1 0	21	100
use 10 2	20	1.000
		10.0
614 E 4	21	0.00
m.c. [] 5		1.8
040K [] *	-	100
MA 7		0400
		0000
H		
940K [] *		9400
		9400 144

Mouse-over graphics to see in larger detail

The main data sheet (link : **si4133.pdf** (http://www.silabs.com/pages/DownloadDoc.aspx? FILEURL=Support%20Documents/TechnicalDocs/si4133.pdf&src=SupportDocLibrary), the standard product) provides a lot of information about typical circuit application as well as the programming requirements. As per my previous synthesiser designs, I contemplated again using the PICAXE series of micro-controllers to set up the control registers using the 3-wire bus arrangement.

The beauty of this chip is that it has two simultaneous independent synthesised RF outputs and requires just a stable reference input clock - somewhere between 2 and 26 MHz - although most applications would probably use 10.000 MHz from an external source such as a TCXO. The "RF1" segment can work from 947 to 1720 MHz as standard, and 1850 to 2050 MHz in extended mode while "RF2" works from 789 to 1429 MHz. Finally, the "IF VCO" can produce RF anywhere from 62.5 to around 1000 MHz by using an actual VCO running from 526 to 952 MHz and being programmed to use internal (/1) /2, /4 or /8 dividers. The VCOs all use external inductors and have a typical range of +5% to -5% of the frequency set by the inductor plus the "centre value" of the internal capacitance (which undoubtedly includes the varicap/varactor tuning diode).

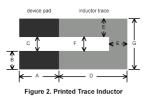
The determination of which one of the RF1 or RF2 segments is active is determined through the programming sequence - if the RF1 values are written last then the RF1 part is active, ditto for the RF2 - written last = active. This means that only one of the RF1/RF2 ports is active at any one time - under software control. The IF port is set up separately so is always active - unless specifically programmed inactive.

The phase detector (PD) will work from 10 KHz to around 1MHz although the higher the PD frequency, the lower the phase noise produced. The quoted typical spec for this is -132 and -134 dBc/Hz at 1 MHz offsets for the RF1 and RF2 ports and -117 dBc/Hz at 100 KHz offset for the IF port. Tests are based on a 200KHz PD.

The basic chip RF output levels are typically 125mV into 50 ohms (around -5dBm) for the IF output (@ 550 MHz) and around 0dBm/50 ohms for the RF1 and RF2 port within their normal range. It is probably good practice to implement an onboard broadband MMIC buffer/amplifier on each output port to raise the level as required, noting that MMICs don't really like a low supply voltage (i.e. such as the +3V for the Si4133) so they should be run from something higher (+5, +8 etc).

The inductance values used at these frequencies are small, small in value and small physically. The maximum value is just 12nH, and that is for the IF VCO down at 526 MHz. It is difficult to actually make a physical inductor with 1nH (yes, a nanoHenry) so it becomes standard fare to create the inductance with a track on the PCB layout - but how do you know how big to make that track ? Read AN31: "Inductor Design For the Si41XX Synthesiser Family" (link : **AN31.PDF** (http://www.silabs.com/pages/DownloadDoc.aspx?

FILEURL=Support%20Documents/TechnicalDocs/an31.pdf&src=SupportDocLibrary)) and it starts to become clear. That document contains details and formulae to allow the user to implement on-PCB inductances. Of course, actually using those formulae to do the calculations is not easy. It was in my interest to use the formulae in a flexible calculator so that I could just enter a desired VCO frequency and the thickness of the PCB material and it would do the rest. A few hours work in MS Excel produced the same results as per the examples in the AN31 document so I knew I was on the right track.



Standard sizes : A = 1.50mm, B = 0.3mm, C = 0.35mm, D = length as calculated (see below), E = 0.30mm, F = 0.2mm, G = 0.8mm

A few sample values calculated for the Si4133-GT chip :

Frequency	External	nH/mm for 1.6mm	Side track length :	Alternate inductor
	Inductance	DS FR4 PCB	Dimension D	arrangement
	Required			
550 MHz	11.25nH	0.7		5nH placed 8.7mm from PCB pins

650 MHz	7.62nH	0.7	10.9mm	5nH placed 3.45mm from PCB pins
750 MHz	5.33nH	0.7	7.61mm	5nH placed 0.17mm from PCB pins
1000 MHz	2.31nH	0.7	3.28mm	N/A
1500 MHz	0.13nH	0.7	0.19mm	N/A

The PCB thickness makes no real difference to the nH/mm value until you use material down around 0.5mm (500uM) thick - or thinner. Please note that if the track width or spacing is varied from those values in the AN31 then the final inductance value per mm will be different. The above formulae is based on AN31's 0.3mm wide rectangular track 0.95mm outer edge to edge (ie. dimensions E & G in the above diagram).

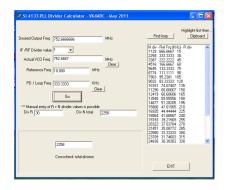
The alternative concept is to make the PCB inductor the longest it can be to work at the lowest frequency for that oscillator (i.e. IF, RF1 or RF2) and then tune the VCO range by soldering a short-circuit part-way along the inductance loop. That makes the RF1 loop at 6.5mm long, RF2 at 8.8mm long and IF at 17.1mm long for double sided 1.6mm FR4 PCB material.

Implementing the above information is a simple as this : If you want the IF VCO to run at 752.666 MHz then you can use an inductor with a 7.6mm length out from the IF chip pins, and "program" the relevant numbers into the chip using a PICAXE (the relevant numbers effectively being R=30, N=2258, giving a PD of 333.3333 KHz - or another set tof divider values to give the correct VCO frequency - see below...) plus the setup coding and it should all work. The alternative to a 5nH SMD inductor (hard to get) is to lay out the PCB so that the side dimension of the inductor track is 7.6mm - so just a PCB inductor and nothing else. A smart person might make it 8 or 9 mm long and solder-bridge the excess !!!

AN31 refers to the Q of the inductor too and specifies it must be > 40. If you are planning on using an external SMD inductor then check the manufacturer's specifications to see what Q they claim. If it isn't high enough, seek another manufacturer or go the track-only PCB style in lieu. It would also be possible to do a helical style but the problem then becomes connecting to the centre on a single-side PCB layout - where the second side is purely ground plane..... Adjusting the inductance may be an issue too.

Oh, how did I get those values for the R and N dividers listed above ? I did a quick re-write of my earlier Delphi-based synthesiser calculator application and put in the divider count limitations of the Si4133 instead. That new application allows me to find what divider values will provide a suitable frequency outcome.

If you look at the graphic below, the RHS "window" shows which "integer-style" (whole number) values will divide into the desired frequency.. The first one is 666.666 KHz with an R divider of 15 giving an N of 1129. The second is 333.333 KHz with an R of 30 and an N of 2258. This second value is the better option simply because it will allow you to step in 333.3333 KHz steps and 753.000 MHz is then just 1 step away (753-752.666 = 333.333 KHz gives N variation of 1). That gives a new N value of 2259. There are no higher-again PD frequencies that will work with the device that will give the desired output frequency.



My alternate requirement is to generate 1627.500 MHz or 1628.000 MHz (frequency doubled = 3255 or 3256 MHz respectively) for use at 3400 MHz and this can be done simultaneously with the IF output still set at 752.666 MHz. That would mean that I could generate the two LO signals for my 2.4 GHz and 3.4 GHz transverters from the one PCB - if they are close enough to each other physically. The highest common R divider value available is 4 (PD=2500KHz) with N values of 651 or 652 respectively und using RF2 VCO, remembering that the higher the PD frequency so the lower the phase noise produced. That PD may be a little high so if we halve it to a value of 1.25MHz, we should still have a low phase-noise result.

I generated my own PCB layout using PCB Express and based the devices on the 24 pin TSSOP Si4133D-GT and a PICAXE 08M - although the PICAXE 14M will also fit on the board. Both of these chips are SMD styles, as are all the remainder of the components used. One thing I must say : these TSSOP chips are SMALL ! This is the first time I have done a layout using one of these and it required a bit of a re-think about track widths. For instance, all tracks going to the TSSOP package can be 0.3mm wide - and that's it.

The PICAXE requires +5V so a 78L05 regulator was used for generating that. The Si4133 has a maximum VDD supply rating of +4V so a simple pass-style NPN regulator was added to supply the 30-odd mA of current required by the synth chip. The 3.9V zener on the base of the NPN pass transistor gives an estimated +3.2v to +3.3v as a supply line. I would have used a 78L03 regulator in an SOT-89 package but these don't seem to be a readily available item. *Post note* : There is now a spot on the revised board layout to take one anyway.

A couple of places were set up on the PCB for the inclusion of MMIC broadband amplifiers on both the RF and IF output sections, but whether these devices are actually required has yet to be seen. If they are - the most likely scenario, the PCB layout is present.

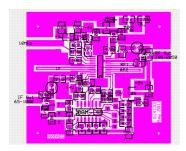
There are on-board PCB-based inductors on each oscillator, the RF1, RF2 and IF, and each has been set to give close to the lowest possible frequency that each VCO can be run at. To run any at a higher frequency requires the placement of a solder bridge across the inductor tracks. The RF1 sized out at 7.5mm long (calculated desired length 6.5mm), RF2 at 10.0mm (calculated desired length 8.8mm) and the IF at 18.5mm (calculated desired length 17.1mm) so all are just a little longer than would be required for operation at the minimum VCO frequency in each case. The length limits are actually due to the size of the physical PCB layout rather than any other factor.

Before you say it, yes, I know that the IF inductor theoretically shouldn't be that long - it should be a shorter track plus fixed SMD value, that track length has to be known before the PCB can be produced - and I may not always know where my experimentation may lead me in terms of operating frequencies !

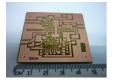
Having these inductors too long means that by judicious placement of a shorting solder "blob", I should be able to move the VCO anywhere within it's allowable tuning range.

I also included a LED option via an inverting transistor (NPN) through a base current limiting resistor off the AUXOUT pin to provide a lock indication arrangement. When AUXOUT = low (VCO locked) then the transistor is off and the LED is off. When the VCO is unlocked, the AUXOUT pin = high, the transistor is saturated lighting the LED. Therefore it is actually an "unlock" indicator.

This is what my layout actually looks like. Yes, it could be neater - and not need any power jumpers - maybe in phase two....

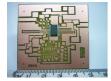


This is my first-run prototype layout of the X-Locker V4, the physical PCB is just 50mm x 45mm. The artwork has been given a few "tweaks" for any further PCBs to be made. All tracks are on the top layer of a double-sided PCB material and the other side remains full copper (i.e. unetched).



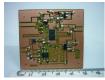
The artwork above translates into this physical PCB.

A few tricks to mention about building up a PCB with a TSS0P24 chip - it isn't super easy and you have to have a hot air tool to do it successfully. A normal soldering iron (even one with a super-fine tip) is just too big. My approach was to tin the 24 pads with some solder, place the chip in the correct position and hold it there while applying hot air evenly along both sides. Once the solder has melted, it will stay there. Examine all pins under a magnifier to ensure that each and every one is a good connection. You need to put this chip on the PCB first since the hot air may de-solder any other parts.



First the Si4133 chip.

The next part added is the SMD-style PICAXE and then the rest of the normal SMD parts are soldered in place. Nothing special to note there, simple item-by-item assembly is all.



Partway through the remainder of the components being added. The two SMA sockets are added last. The 10MHz TCXO connection was made by miniature coax for testing.

The PCB I built up uses a PICAXE 08M so does not require all of the pull-up resistors shown on the layout to be fitted. It also requires that the first command in the code establishes the "function pins" 1, 2 and 4 as outputs - note that in practice, the physical pins numbers are 3, 5 and 6. This command is not required on a 14M as the pins are already set as outputs.



There are quite a few PCB pads not used when the 08M PICAXE is used, down at the middle bottom of the image. This photo was taken after "tuning" the VCO inductor lengths - the solder "blob" positions are reasonably obvious.

The final software is a mix of a version supplied directly by David VK3HZ and mine. It sets up both the RF1 and IF ports to produce 1627.500 and 752.6666 MHz respectively and the resulting configuration produces levels of about -1dBm and -5dBm respectively without any MMIC amplifiers installed. These RF levels are very close to the published specs values.

The original software made a single pass through the code and set up just one VCO, my variant does a double-pass setting up a different VCO each time (i.e. RF1 or RF2 and then the IF, or they can be done in the reverse order). After the second pass, it waits in a loop to see if the jumper setting on pin 4 of the PICAXE is changed and reprograms the frequencies as required.

One of the issues with PICAXEs like the 08M and 14M is the limited memory for the active program. For instance, the 08M has a space for tokenised instructions of just 256 bytes so code efficiency is paramount.

The target levels for most transverter board LO inputs is around +10dBm so that means we should include a MMIC amplifier with a gain of around 12dB at 1.7GHz on RF1/2 output (e.g. an ERA4, 14dB) and 15 to 16dB at 750 MHz on the IF port (e.g. an ERA2, 16dB). Both of these devices have a 1dB compression output point above +10dBm - our target. Of course, we can always insert some output attenuation if the level is too high....

David's implementation requires the values for the various synth registers to be set up in an array in the EEPROM of the PICAXE and while he sent me up a copy of an Excel calculator for these values, when I tried it with some weird (well, weird for many others) values, it fell over. I extracted the formulae and implemented a stand-alone Windows application that would calculate the values in a format to suit his coding.

🖅 Si4133 Calc for VK3HZ softw	are	
Ref 10.0000 NHz	Any box with a yellow background can be changed	Rel Divisor Check
PD 0.3333333333333333 MHz	R Divider 30 0001E0	R · PD Freq (KHz) 15 : 666.66670000 20 : 333.33300000 45 : 222.222200000
VCO 752 BESEBEEBEE MHz	N Divider 2258 008D20	60 : 166.666700000 90 : 111.111100000 105 : 95.238100000
Calo NOTE : ALL VALUES PREFIXED	BY \$ FOR ENTRY INTO THE EEPROM TABLE	120 : 83.333330000 135 : 74.074070000 180 : 55.555560000 210 : 47.61965000
NM 00	NI NL 8D 23 RF1	270 : 37.037040000 285 : 35.087720000 315 : 31.746030000
	24 BF2 25 IF	360 - 27.777780000 405 - 24.631350000 420 - 23.89550000 480 - 20.83330000 540 - 18.51850000
BM 00	RI RL RF1	570 : 17.543860000 630 : 15.873020000 720 : 13.888890000 810 : 12.345680000
	E7 RF2	840 : 11.904760000 855 : 11.695910000 945 : 10.582010000
	E8 IF	960 : 10.416670000 1090 : 9.259259000
VK44DC 2011 - Note : not a lot	of error trapping	1095 : 9.132420000

The above graphic shows the setup details required for the first frequency in the lower part of the screen. The ZIP containing the Si4133V3.EXE file can be downloaded here (/~vk4adc/web/images/UserFiles/File/datafiles/Si4133V3.zip) (166KB zip).

The first 4 EEPROM locations were set up so that they configured :

1:1627.5000 on RF1

2:753.0000 on IF

3: 1628.000 on RF1

An extract from the actual code looks like this ...

...

' 08M note : only 4 sets of data are required as there is only 1 alternate frequency jumper input, and two VCOs are set up together

' Use VK4ADC's Windows application to easily calculate the values below.

' NM NI NL RM RI RL	
1	
eeprom (\$00, \$8D, \$25, \$00, \$01, \$E8)	'0 - 752.666 MHz, IF, PD = 333.333 KHz
eeprom (\$00, \$51, \$63, \$00, \$00, \$86)	'1 - 1627.500 MHz, RF1, PD = 1 MHz
eeprom (\$00, \$2F, \$15, \$00, \$00, \$A8)	'2 - 753.000 MHz, IF, PD = 1 MHz
eeprom (\$00, \$65, \$C3, \$00, \$00, \$A6)	'3 - 1628.000 MHz, RF1, PD = 1 MHz

If the board is powered up normally (no jumper), the first two frequencies are generated (using locations 0 & 1 : 752.666 and 1627.5000) but if the jumper to ground is present on pin 4 of the PICAXE 08M, then the second set is used (locations 2 & 3 : 753.000 and 1628.000). This allows the board to be used for an IF of 145.0 MHz without the jumper and 144.0 with it (assumes 2403.0 and 3400.0 band edges, frequency tripling in the 2400 transverter LO chain and frequency doubling in the 3400 one.). Of course, other frequencies could be set up in place of these. The code re-checks that external jumper state and updates the selections automatically.

The tuning of the printed circuit inductors is a tricky process. The PICAXE was set up to re-program the Si4133 for a series of frequencies at 100 MHz intervals from 500 MHz to 1900 MHz and a "shorting blob" was soldered across the inductors in turn while monitoring the relevant outputs with a frequency counter. When the VCO locked, the counter would display the generated frequency & by "shifting" where the blob was, I was able to get a suitable VCO range to operate the chip at 750, 1200 and 1600 MHz somewhere towards the middle of each lock range. Be warned : it took me a couple of hours experimenting with positions - it was not a "cut & dried" process - so expect something similar.

Every circuit board is likely to produce different values (to an extent) so quoting exact measurements isn't going to help too many synthesiser 'duplicators' however the RF1 blob is around 1mm from the pins, the RF2 is at around 4.5mm from the side of the package and the IF one is around 7mm from the side of the package. It is difficult to get the blob right next to the RF1 pins without actually joining them at the pins - the solder just flows there. Note that two different references are used in the position descriptions above - from the pins for RF1 and from the side of the package for the RF2 and IF inductors

David suggested incorporating a "clean-up filter" on the 10MHz clock input (as used in the DEMI synths using this same chip) and there is space on the PCB layout for its inclusion. I may also include a level-setting trimpot so that it can be adjusted as required because one of my TCXOs actually has too high a level and the synth won't lock with it connected, although locking isn't an issue with my second TCXO and GPSDO. My CRO tells the story : the first TCXO has quite a high output level in comparison to the other two... The cleaner your 10.000 MHz reference is, the cleaner the output signal !!

Post-note : The artwork has been altered around the 10 MHz input so that a Pi-network low pass filter can be inserted, as can a 100 ohm 4mm trimpot to adjust the level - both of these component segments are optional.

Listening to the synthesiser signal on a receiver indicated there was a crisp heterodyne as the tuning of the receiver was swept across it (in USB mode) and very little phase noise was evident/heard. Not definitive by any means but still good as a comparative guide.

The two MMIC amplifiers were then added to increase the output level to around +10dBm... Actually, I had a quantity of ERA5's available so put one in each place (bias resistor of 47 ohms for +8v, 120 ohms for a +12v supply). The result was +14dBm at 1627.5 MHz and just over +13dBm at 752.66 MHz. I later found that the power supply voltage was high - up around +12V, and while not damaging, the MMIC's output levels were higher than they should have been. The levels are close to +10dBm on both ports at +8V supply.

Post-note : The artwork has been altered around the two outputs, IF and RF1/2 to allow the insertion of a Pi-network attenuator on each port to adjust levels. These parts can be left out if desired.

The FAQ's for the Si4133 recommend a shielded enclosure so I fabricated 4 separate side pieces from tinplate and soldered them to both the top and bottom of the PCB (see photo), as well as up each seam. The SMA sockets were soldered on the outside with the centre conductor pin passing through a 3.5mm hole in the tinplate at the relevant points to connect to the PCB tracks - note : drill the holes before soldering the sockets into place.



This is the completed synthesiser, just 51mm x 46mm in size, 21mm thick, with the tinplate shielding soldered on the 4 sides. The SMA connectors are : Top LHS - 10 Mhz in, Bottom LHS - 752.666 MHz out, Top RHS - 1627.500 MHz out. The PTFE pin at bottom RHS is the +8V power input. The four 3mm holes in the 4 corners of the PCB will take screws down into threaded metal standoffs for mounting. The green-bodied components are 1.5uH axial RFCs that do double duty : (1) feed +8V DC to the relevant points; and (2) provide a little RF isolation along the supply leads.



The underside view shows the tinplate sides are soldered all around the outside of the PCB, underneath as well as inside. The corner mounting holes are a little easier to see in this view. All of the soldered joints (other than along the sides) are wired-through "vias".

I also fabricated a tin lid to close off the top, the bottom already being sealed off by virtue of the un-etched PCB material on the bottom side.



The side view of the box shows the tinplate panels a little clearer. The lid to fit over the assembly is at right.



With the lid fitted.

A final warning : If you are using the Si4133**G**-GT chips, you can use the same code as for the standard Si4133D-GT chip however the R divider will always be 65 (= 153.846153846154 KHz) so that needs to be used in the synthesiser calculator software. It means that there are a lot of frequencies that you cannot achieve access to (eg only EVEN MHz values can be generated (i.e. at intervals of PD * 13), not ODD MHz and nothing that isn't a multiple of the 153.xxx KHz PD frequency !!)

CODE :

The "final" version of the PICAXE 08M code to suit my application of the Si4133 is available here (/~vk4adc/web/images/UserFiles/File/datafiles/S4133_Loader_08M.zip) as a ZIP file. Of course, it needs to be edited if used for different frequencies.....

Sorry, I am not giving away the actual Schematic or PCB files.... although most of the component details can be gleaned from the PCB overlay above if you are willing to work for it. I have coined the term "X-Locker V4" for this project as a continuation of the synthesiser development projects.

USE : There are a lot of possible projects that could use this sythesiser - basically anything that needs a LO signal anywhere between about 60 MHz and 2.05 GHz.

A few immediate examples are the work to stabilise a 2.4 GHz Down East Microwave transverter (/~vk4adc/web/index.php/microwave-projects/63-transverters/144-demi-13cm-lo-update.html). Alternatively, both a W1GHZ 2.4 GHz transverter (/~vk4adc/web/index.php/microwave-projects/63-transverters/142-building-a-w1ghz-based-13cm-transverter.html) and the W1GHZ 3.4GHz model (/~vk4adc/web/index.php/microwave-projects/63-transverters/143-building-a-w1ghz-based-9cm-transverter.html) running similtaneously from one synth board.

It could also be the frequency source for a beacon transmitter for the 2.4, 3.4, 5.7 or 10GHz - and all derivable from a 10MHz frequency reference like a GPSDO so ultra-stable.